AN10830

Interconnection between JESD204A compliant devices

Rev. 2 — 23 September 2010   **Application note**

Document information

Info	Content
Keywords	JESD204A, Data converters, CML, LVDS, Jitter, Coupling
Abstract	This document describes the interconnections that are required between the data converter device and the logic device for a JESD204A standard compliant system. It also depicts the types of interface that are necessary for the various signals.

Revision history

Rev	Date	Description
2	20100923	Second, updated issue
1	20090528	First issue

Contact information

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1. Introduction

The JDEC JESD204A is a serial interface standard dedicated to data converters. It has been defined by all the major stakeholders in the industry, involving System integrators, IC suppliers (including NXP Semiconductors) and Field Programmable Gate Array (FPGA) producers. This ecosystem is very useful as it allows easy interoperability between IC providers and FPGA makers.

Its main purpose is to simplify PCB design and facilitate longer transmissions with guaranteed integrity.

NXP Semiconductors offer the following JESD204A compliant devices, as part of its portfolio:

- DAC1408D650 14-bit dual DAC, JESD204A compliant, 650 Msps maximum output rate; see Ref. 1 "Data sheet DAC1408D650"
- DAC1408D750 14-bit dual DAC, JESD204A compliant, 750 Msps maximum output rate; see Ref. 2 "Data sheet DAC1408D750"
- ADC1413D 14-bit dual ADC, JESD204A compliant, f_s = 125 Msps, 105 Msps, 80 Msps and 65 Msps; Ref. 3 "Data sheet ADC1413D series"
- ADC1213D 12-bit dual ADC, JESD204A compliant, f_s = 125 Msps, 105 Msps, 80 Msps and 65 Msps Ref. 4 "Data sheet ADC1213D series"
- ADC1113D 11-bit dual ADC, JESD204A compliant, f_s = 125 Msps Ref. 5 "Data sheet ADC1113D125"
- ADC1413S 14-bit single ADC, JESD204A compliant, f_s = 125 Msps, 105 Msps, 80 Msps and 65 Msps Ref. 6 "Data sheet ADC1413S series"
- ADC1213S 12-bit single ADC, JESD204A compliant, f_s = 125 Msps, 105 Msps, 80 Msps and 65 Msps Ref. 7 "Data sheet ADC1213S series"

Xilinx Virtex5 documentation is available from: http://www.xilinx.com/. Documents of interest are UG196 *(Virtex-5 FPGA RocketIO GTP Transceiver)* and DS202 *(Virtex-5 FPGA Data Sheet: DC and Switching Characteristics)*. This application note does not intend to replace these.

JESD204A has been issued by the JEDEC committee. This specification can be downloaded from the web site http://www.jedec.org/. NXP also provides an application note (*AN10812_1, JESD204A: New serialization technology for high speed data converters*) to give the customer sufficient background on that standard.

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## 2. Efficiently connecting NXP Semiconductors JESD204A DAC to Xilinx FPGA
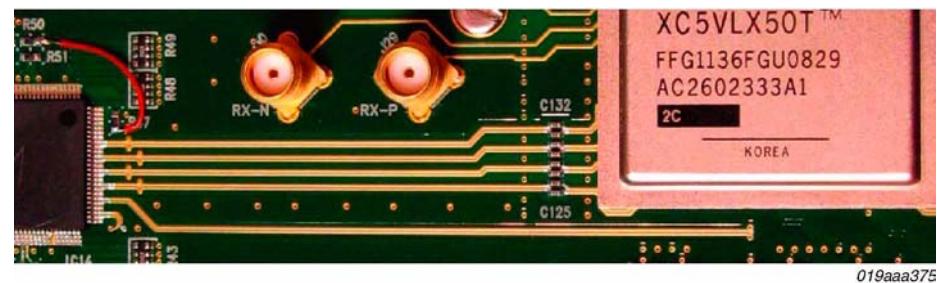
Fig 1.   Lane interconnect example

JESD204A is a point-to-point protocol. There are three categories of connections:

- **Lanes**: Carry the data.
- **SYNC**: This is a synchronization signal used at the beginning of the transmission. It is also used by the receiver to trigger loss of synchronization and requests reinitialization.
- **Frame clock**: This is the system clock.

2.1 Virtex5 FPGA

The key feature that these devices require is a SerDes macro. It ensures the proper serialization/deserialization of the data at very high speeds. Moreover, they have extra features such as Phase Locked Loops (PLL) running at very high frequencies (> 1 GHz) and hard wired 8b/10b coding/decoding.

In Xilinx terminology, these highly specialized macros are named GTP or GTX depending on their characteristics. The commercial name used is RocketIO. All Virtex5 devices, with part numbers ending "T", contain such transceivers (eg XC5VLX50T, XC5VFX70T, etc.). GTP and GTX have a fixed location inside the FPGA. This is an important point for board design strategy.

2.2 Lanes

JESD204A specifies that the data link should be Current Mode Logic (CML) compliant. This implies current switching with the positive supply, V_{DD} as reference. This also means that each lane is made up of a differential pair. The termination level on both sides of the link is set to 50 Ω.

As V_{DD} is the reference, special care must be taken when the transmitter (an FPGA) and receiver (an NXP Semiconductors DAC) have different supply voltages. This can lead to different common-mode voltages on each side, thus creating a potential difference. JESD204A has introduced the concept of AC or DC coupling to avoid different common-mode voltages on each side. This prevents static current from flowing from one device to the other.
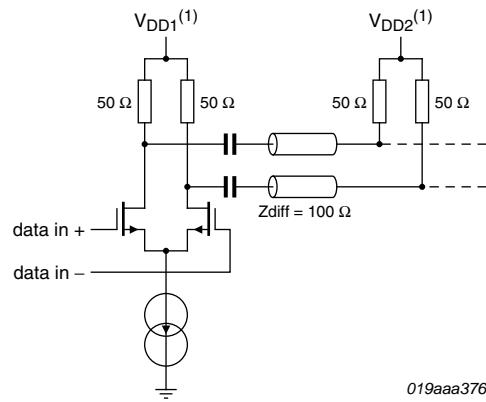
Fig 2.   AC coupling
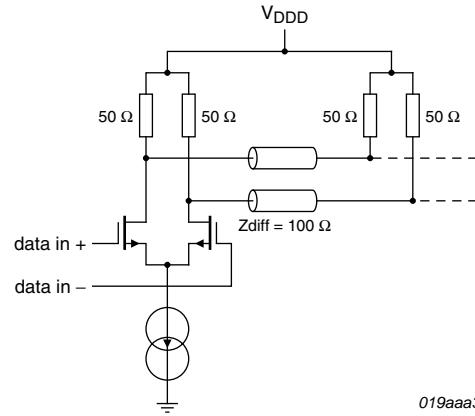
Fig 3.   DC coupling

The AC coupling capacitor and the load resistors create a high pass filter. The value of the capacitor determines the lower cut-off frequency of this first order filter. A 10 nF capacitor is sufficient to ensure correct AC coupling, as the cut-off frequency is at 0.3 MHz and is therefore not seen by the high frequency signals.

Example: The NXP Semiconductors DAC1408D650 demoboard features a DAC1408D650 and an XC5VLX50T. The DAC1408D has a default common-mode voltage of 800 mV. Virtex5 GTP has a common-mode voltage of 800 mV, so no capacitor is required. The DAC1408D650 has a configurable common-mode voltage, which covers a range of 700 mV to 1400 mV if another device is used.

2.3 Frame clock

This clock must be provided to the FPGA and to the data converter device. They must have the same frequency but the phase relationship can have any value (e.g. 180 °).
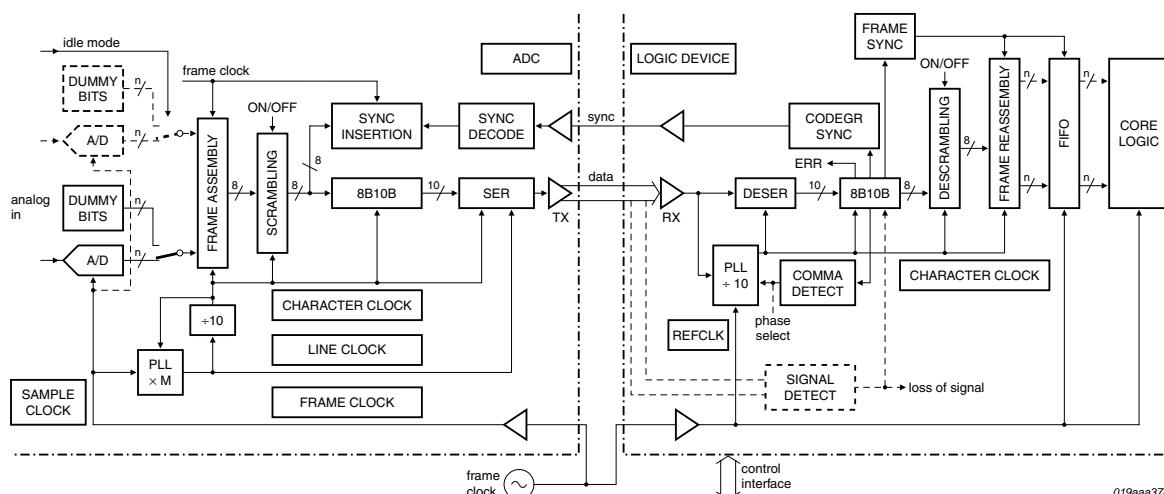

Fig 4.   System description of the JESD204A with clock distribution

All clocks are based on the frame clock, which is the absolute timing reference in the JESD204A system. It is a relatively low frequency clock which is also the sampling clock of the ADC or the DAC. It is distributed as a separate signal and supplied to all transmitter and receiver devices in the pipe.

The JESD204A transmitter and receiver must first synchronize through the SYNC interface. This interface is used as a time-critical return path from the receiver(s) to the transmitter(s). It is synchronous with the frame clock input of the devices.

The JESD204A data interface guarantees the synchronization between different devices. This allows for good matching between data lanes, which is very beneficial for the interoperability between FPGA vendors.

As mentioned in Section 2.1 an 8b/10b coding is used to encode data before transmission. The 8b/10b codes have the following properties:

- The global clock network
- The dedicated macro input

Xilinx recommends the dedicated macro input for best jitter performances.

This dedicated input is differential. It is very similar to CML and is terminated by a 50 Ω resistor to a common-mode voltage. Driving these pins directly is only possible with a driver that has the same common-mode voltage. Otherwise, bypass capacitors must be set up on the nets.

When a clock is provided to the ADC device, it should be in a suitable differential interface, LVDS, LVPECL, SINE or LVCMOS. It is the sampling clock and it will influence the quality of the ADC.

2.4 Convertisseur Grande Vitesse (CGV) implementation

CGV designates NXP Semiconductors compliant, superset implementation of the JEDEC JESD204A interface standard, with an enhanced rate (4.0 Gbps typical), an enhanced reach (100 cm typical), enhanced features (multiple DAC synchronization) and an assured FPGA interoperability. NXP Semiconductors offers enhancements in terms of transceiver rate (up to 4.0 Gbps against the standard rate of 3.125 Gbps, a 28 % increase) and transmitter reach (up to 100 cm versus the standard reach of 20 cm, a 400 % increase). The enhanced CGV features include Multi Device Synchronization (MDS), which is not specified, but informatively discussed in the JEDEC specification. NXP Semiconductors has implemented this optional feature to enable LTE MIMO base stations and other advanced multichannel applications. The NXP Semiconductors implementation of MDS enables up to sixteen DAC data streams to be sample synchronized and phase coherent.

2.5 Layout

Two types of buses are required to interconnect NXP Semiconductors JESD204A data converter device and a Virtex5:

- LVDS
- CML

2.5.1 LVDS routing

LVDS signaling has very fast edges. Use differential routing with controlled impedance. Impedance discontinuities must be avoided as they create high frequency spurs, which can create noise when coupled to the rest of the circuit.

Target impedance is 100 Ω differential.

2.5.2 CML routing

The same layout constraints as for LVDS apply here. Target impedance is also 100 Ω differential.

Both the NXP Semiconductors JESD204A DAC and the Virtex5 FPGA have lane polarity swapping capability to ease PCB routing. This allows the differential pairs to be routed in the most direct way possible and the polarity issue to be dealt with very easily.

3. References

[1] **Data sheet DAC1408D650 —** Dual 14-bit DAC; up to 650 Msps; 2×, 4× or 8× interpolating

[2] **Data sheet DAC1408D750 —** Dual 14-bit DAC; up to 750 Msps; 2×, 4× or 8× interpolating

[3] **Data sheet ADC1413D series —** Dual 14-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps; serial JESD204A interface

[4] **Data sheet ADC1213D series —** Dual 12-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps

[5] **Data sheet ADC1113D125 —** Dual 11-bit ADC; serial JESD204A interface

[6] **Data sheet ADC1413S series —** Single 14-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps; serial JESD204A interface

[7] **Data sheet ADC1213S series —** Single 12-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps

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